Amendments to the Claims:

The following claims will replace all prior versions of the claims in this application (in the unlikely event that no claims follow herein, the previously pending claims will remain):

1-6. (Cancelled)

7. (Currently Amended) A method for fabricating a semiconductor memory device including a cell region and a peripheral circuit region, the method comprising ~~the steps of~~:

forming a plurality of line patterns in the cell region and the peripheral circuit region, each being formed by stacking a conductive layer, ~~and~~ an insulating hard mask, and a spacer allocated at sidewalls of each of the line patterns;

removing the entire insulating hard mask and the entire spacer formed in the peripheral circuit region;

forming a conductive spacer at sidewalls of each line pattern in the peripheral circuit region, wherein a spacing distance between the line patterns is at least onefold greater than a width of the line pattern;

forming an insulation layer on an entire surface of the resulting structure;

forming a photoresist pattern for forming a contact hole exposing the conductive layer on the insulation layer; and

forming a deep contact hole exposing the conductive layer by etching the insulation layer with use of the photoresist pattern as an etch mask.

8. (Original) The method as recited in claim 7, wherein the line pattern in the peripheral circuit region has a ratio of a width to a spacing distance in a range of about 1:1.05 to about 1:1.30.

9. (Original) The method as recited in claim 7, wherein a ratio of a width of the line pattern to a spacing distance between line patterns in the cell region is about 1:1.

10. (Currently Amended) The method as recited in claim ~~6~~ 7, wherein a ratio of the width of the line pattern in the cell region to that of the line pattern in the peripheral circuit region is in a range of about 1:1 to about 1:1.3.

11. (Currently Amended) The method as recited in claim ~~6~~ 7, wherein the conductive spacer is made of any material selected from a group consisting of TiN, TaN, W or WN.

12. (New) The method as recited in claim 7, wherein the spacer is formed with one of a silicon nitride layer and a silicon oxide nitride layer.

13. (New) The method as recited in claim 7, wherein the conductive layer is made of any material selected from a group consisting of W and TiN.

14. (New) The method as recited in claim 7, wherein the insulating hard mask is formed with one of a silicon nitride layer and a silicon oxide nitride layer.

15. (New) The method as recited in claim 7, wherein the insulating hard mask is removed by a photoresist strip process.